REMARKS

After entry of this amendment, claims 61-80 remain pending. In the present Office Action, claims 61-72 were rejected under 35 U.S.C. § 102(b) as being anticipated by Baum, U.S. Patent No. 5,303,358 ("Baum"). Claims 73-80 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Baum in view of Gulick et al., U.S. Patent No. 5,732,224 ("Gulick"). Applicants respectfully traverse these rejections and request reconsideration.

Claims 61-80

Applicants respectfully submit that each of claims 61-80 recite combinations of features not taught or suggested in the cited art. For example, claim 61 recites a combination of features including: "the execution core is configured to...use the value of the register address field to select one of *either* a least significant portion *or* a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register". Neither Baum, nor Baum in view of Gulick, teach or suggest the above highlighted features.

With regard to the features "the execution core is configured to...use the value of the register address field to select one of *either* a least significant portion *or* a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers", the Office Action refers to Baum, col. 1, line 66-col. 2, line 6; col. 3, line 67-col. 4, line 15; Figures 2B and 2C; and col. 5, lines 5-19 and 31-41. However, col. 1, line 66-col. 2, line 6 generally describes a prefix instruction and its use in modifying the following (or "using") instruction, and particularly discusses identifying

a register that stores the result or supplies an operand using the prefix instruction. However, these broad teachings do not teach or suggest the above highlighted features. Col. 3, line 67-col. 4, line 15 teaches that various instructions operate on 32-bit words, 16-bit halfwords, 8-bit bytes, and individual bits, and describes Figs. 2b and 2c as illustrating the position of halfwords and bytes within a word. However, there is no teaching regarding how halfwords and bytes are accessed within a register for a given instruction. Therefore, there is no teaching that "the execution core is configured to...use the value of the register address field to select one of *either* a least significant portion *or* a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers" as recited in claim 61. Finally, Fig. 3, col. 5, lines 5-19 and 31-41 of Baum teach the use of a prefix instruction to provide an extra register designation that can be used as a destination register or a source operand. However, these teachings again do not teach or suggest "the execution core is configured to...use the value of the register address field to select one of *either* a least significant portion *or* a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers" as recited in claim 61.

Nevertheless, Applicants have further clarified claim 61, reciting: "a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register". Baum appears to include no teaching that a first value encoded in the register address field results in selection of different portions of different registers dependent on whether or not the instruction includes the prefix field.

For at least all of the above reasons, Applicants submit that claim 61 is patentable over the cited art. Claims 62-64 depend from claim 61, and thus are patentable over the

cited art for at least the above stated reasons as well. Each of claims 62-64 recites additional combinations of features not taught or suggested in the cited art.

Claim 65 recites a combination of features including: "the processor is operable to ... use the value of the register address field to select one of either a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register". The teachings of Baum, highlighted above with regard to claim 61, also do not teach or suggest the above highlighted features of claim 65. Accordingly, Applicants submit that claim 65 is patentable over the cited art. Claims 66-68 depend from claim 65, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 66-68 recites additional combinations of features not taught or suggested in the cited art.

Claim 69 recites a combination of features including: "responsive to detecting a lack of the prefix field in the instruction, selecting either a least significant portion or a second least significant portion of one of a subset of the plurality of registers dependent on the value of the register address field, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register". The teachings of Baum, highlighted above with regard to claim 61, also do not teach or suggest the above highlighted features of claim 69. Accordingly, Applicants submit that claim 69 is patentable over the cited art.

Claims 70-72 depend from claim 69, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 70-72 recites additional combinations of features not taught or suggested in the cited art.

Claim 73 recites a combination of features including: "the processor is configured to ... use the value of the register address field to select one of either a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register". The teachings of Baum, highlighted above with regard to claim 61, also do not teach or suggest the above highlighted features of claim 73. Gulick is relied on to alleged teach a peripheral device, and does not teach or suggest the above highlighted features, either. Accordingly, Applicants submit that claim 73 is patentable over the cited art. Claims 74-80 depend from claim 73, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 74-80 recites additional combinations of features not taught or suggested in the cited art.

Drawing Objection

The present Office Action objected to Fig. 2, stating that the alignment of 15, 16, and 31 is confusing. Applicants respectfully disagree and submit that Fig. 2 is clear as filed, particularly in light of the specification. Nevertheless, Applicants have amended Fig. 2 so that 15, 16, and 31 are shown horizontally. Applicants believe that no new matter has been entered.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested. If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-66100/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☒ Other: 1 Replacement drawing sheet (Fig. 2)

Respectfully submitted,

Lawrence J. Merkel
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AGENT FOR APPLICANT(S)

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Date: 3/8/05

IN THE DRAWINGS:

Attached hereto is 1 replacement drawing sheet, replacing Fig. 2 as currently on file. Changes to the drawing are described below.